CLAIMS

What is claimed is:

1. An apparatus for setting an overflow flag based on a shift value and input data for one of a plurality of operations executed in a bit manipulation unit (BMU), the apparatus comprising:

a first logic circuit, for a first subset of the plurality of operations, setting a first overflow value based on the left shift value and the input data;

a second logic circuit, for a second subset of the plurality of operations, setting a second overflow value based on the right shift value and the input data; and

a selector providing either the first or the second overflow value as the overflow flag based on a signal identifying the one of the plurality of operations executed by the BMU.

2. The invention as recited in claim 1, wherein the first logic circuit sets the first overflow value by:

1) comparing a number of redundant sign bits to a combination of the number of most significant bits (MSBs) of the input data and the shift value, and

2) setting the first overflow value based on the comparison, wherein

the most significant bits correspond to bits at positions for a set of guard bits in the input data and at least one bit of the input data.

3. The invention as recited in claim 2, wherein the first logic circuit comprises:

a saturator forming the combination; and

an exponent and compare module comparing the number of redundant sign bits based on the combination.

4. The invention as recited in claim 1, wherein the second logic circuit sets the second overflow value by:

1) comparing the number of redundant sign bits to a combination of the most significant bits of the input data and the shift value, and

2) setting a second overflow value based on the comparison, wherein

the most significant bits correspond to bits at positions for a set of guard bits in the input data and at least one bit of the input data.

5. The invention as recited in claim 4, wherein the second logic circuit comprises:

an exponent module generating an exponent for the input data, the exponent module including means for prepending a sign to the exponent to generate a value corresponding to the number of redundant sign bits;

a combiner adding the shift amount to the value corresponding to the number of redundant sign bits to form a combined value;

a comparator generating the comparison as the difference between the combined value and the number of most significant bits of the input data.

6. The invention as recited in claim 1, wherein the apparatus is a circuit, and wherein:

the first logic circuit comprises:

a saturator forming a combination of the number of most significant bits (MSBs) of the input data and the shift value, the most significant bits corresponding to bits at positions for a set of guard bits in the input data and at least one bit of the input data; and

an exponent and compare module comparing a number of redundant sign bits based on the combination, exponent and compare module setting the first overflow value based on the comparison; and

the second logic circuit comprises:

an exponent module generating an exponent for the input data, the exponent module including means for prepending a sign to the exponent to generate a value corresponding to a number of redundant sign bits;

a combiner adding the shift amount to the value corresponding to the number of redundant sign bits to form a combined value;

a comparator generating the comparison as the difference between the combined value and the most significant bits of the input data, wherein the second overflow value is set based on the comparison.

7. The invention as recited in claim 1, wherein the apparatus is embodied as a circuit.

8. The invention as recited in claim 7, wherein the circuit is embodied in an integrated circuit.

9. The invention as recited in claim 1, wherein the apparatus is embodied in either a digital signal processor, microprocessor, micro-controller, or application-specific integrated circuit.

10. A method of setting an overflow flag based on a shift value and barrel-shifted input data for one of a plurality of operations executed in a bit manipulation unit (BMU), the method comprising the steps of:

(a) for a first subset of the plurality of operations, setting a first overflow value based on the left shift value and the input data;

(b) for a second subset of the plurality of operations, setting a first overflow value based on the right shift value and the input data; and

(c) selecting either the first or the second overflow value as the overflow flag based on a signal that identifies the one of the plurality of operations executed by the BMU.

11. The invention as recited in claim 10, wherein step (a) comprises the steps of:

(a1) comparing a number of redundant sign bits to a combination of the number of most significant bits of the input data and the shift value, wherein the most significant bits correspond to bits at positions for a set of guard bits in the input data and at least one bit of the input data, and

(a2) setting the first overflow value based on the comparison;.

12. The invention as recited in claim 10, wherein step (b) comprises the steps of:

(b1) comparing a number of redundant sign bits to a difference between most significant bits of the barrel-shifted input data and the shift value, wherein the most significant bits correspond to bits at positions for a set of guard bits in the input data and at least one bit of the input data, and

(b2) setting a second overflow value based on the comparison.

13. The invention as recited in claim 10, wherein the method is embodied in a processor in an integrated circuit.

14. The invention as recited in claim 10, wherein the method is embodied in a processor of either a digital signal processor, microprocessor, micro-controller, or application-specific integrated

circuit.

15. A computer-readable medium having stored thereon a plurality of instructions, the plurality of instructions including instructions which, when executed by a processor, cause the processor to implement a method for setting a overflow flag based on a shift value and barrel-shifted input data for one of a plurality of operations executed in a bit manipulation unit (BMU), the method comprising the steps of:

(a) for a first subset of the plurality of operations, setting a first overflow value based on the left shift value and the input data;

(b) for a second subset of the plurality of operations, setting a second overflow value based on the right shift value and the input data; and

(c) selecting either the first or the second overflow value as the overflow flag based on a signal that identifies the one of the plurality of operations executed by the BMU.